CLAIMS

What is claimed is:

1. A memory comprising:

an array of memory cells formed in rows and columns;

a sense amplifier coupled to the array of memory cells, the sense amplifier having a first input for receiving a current corresponding to a data value from one of the memory cells, a second input for receiving a predetermined reference current and an output for providing an output data value when the memory is read; and

read control circuitry coupled to the second input of the sense amplifier, the read control circuitry having a reference transistor for providing the predetermined reference current in response to a reference voltage, the read control circuitry varying the reference voltage in a manner to maintain the predetermined reference current at a substantially constant value.

2. The memory of claim 1 wherein the array of memory cells is comprised of transistors having nanoclusters and the reference transistor is comprised of a transistor that does not have nanoclusters.

3. The memory of claim 2 wherein the nanoclusters further comprise silicon nanocrystals.

4. The memory of claim 3 wherein the read control circuitry has an input coupled to the second input of the sense amplifier for biasing the reference transistor in response to variation of the reference current caused by numerous program and erase cycles.

5. The memory of claim 1 wherein the current corresponding to the data value provided by the array of memory cells varies as a function of a number of program and erase cycles of the memory, and the reference transistor is programmed and erased a same number of times as the array of memory cells.

6. The memory of claim 5 wherein the read control circuitry further provides a first control signal and a second control signal as values that respectively apply a substantially same gate voltage to the reference transistor and an addressed memory cell of the array of memory cells in response to receiving a read enable signal.

7. The memory of claim 6 wherein the read control circuitry makes the gate voltage of the reference transistor and the addressed memory cell of the array of memory cells to be different values in response to the read enable signal not being asserted.

8. The memory of claim 1 wherein the read control circuitry further comprises a first control signal for controlling a value of the reference voltage and a second control signal for controlling a value of a read voltage applied to the array of memory cells.

9. A method for extending operating life of a memory comprising:

providing an array of memory cells formed in rows and columns;

coupling a sense amplifier to the array of memory cells, the sense amplifier having a first input for receiving a current corresponding to a data value from one of the memory cells, a second input for receiving a predetermined reference current and an output for providing an output data value when the memory is read; and

coupling read control circuitry to the second input of the sense amplifier, the read control circuitry having a reference transistor for providing the predetermined reference current in response to a reference voltage, the read control circuitry varying the reference voltage in a manner to maintain the predetermined reference current at a substantially constant value.

10. The method of claim 8 further comprising implementing the array of memory cells with transistors having nanoclusters and implementing the reference transistor with a transistor that does not have nanoclusters.

11. The method of claim 8 further comprising varying the current corresponding to the data value provided by the array of memory cells as a function of a number of program and erase cycles of the memory and programming the reference transistor erasing the reference transistor a same number of times as the array of memory cells.

12. The method of claim 8 further comprising biasing the reference transistor in response to variation of the reference current caused by numerous program and erase cycles.

13. The memory of claim 8 further comprising controlling a value of the reference voltage and controlling a value of a read voltage applied to the array of memory cells.

14. The memory of claim 8 further comprising applying a substantially same gate voltage to the reference transistor and an addressed memory cell of the array of memory cells in response to receiving a read enable signal.

15. The memory of claim 8 further comprising making a gate voltage of the reference transistor and the addressed one of the array of memory cells to be different values in response to the read enable signal not being asserted.

16. A memory comprising:

an array of memory cells formed in rows and columns;

sense amplifier means coupled to the array of memory cells, the sense amplifier means having a first input for receiving a current corresponding to a data value from one of the memory cells, a second input for receiving a predetermined reference current and an output for providing an output data value when the memory is read; and

read control circuitry means coupled to the second input of the sense amplifier means, the read control circuitry means having a reference transistor for providing the predetermined

reference current in response to a reference voltage, the reference transistor having a threshold voltage that varies to a number of times the reference transistor is biased, the read control circuitry means varying the reference voltage in a manner to maintain the predetermined reference current at a substantially constant value.

17. The memory of claim 16 wherein the read control circuitry means has an input coupled to the second input of the sense amplifier for biasing the reference transistor in response to variation of the reference current caused by numerous program and erase cycles.

18. The memory of claim 16 wherein the current corresponding to the data value provided by the array of memory cells varies as a function of a number of program and erase cycles of the memory, and the reference transistor is programmed and erased a same number of times as the array of memory cells.

19. The memory of claim 16 wherein the read control circuitry means further provide a first control signal and a second control signal as values that respectively apply a substantially same gate voltage to the reference transistor and an addressed one of the array of memory cells in response to receiving a read enable signal.